WHAT IS CLAIMED IS:

1. A phase-change memory device comprising:

a phase-change material layer and a first electrode having a contact area therebetween that extends into a recess of the first electrode to provide current density concentration adjacent thereto.

2. The phase-change memory device of claim 1, wherein a portion of the phase-change material layer extending into the recess of the first electrode comprises a tapering tip of a vertical part of the phase-change material layer that contacts the first electrode at the contact area.

3. The phase-change memory device of claim 2, wherein the phase-change material layer further includes a horizontal part extending above the vertical part and wherein the phase-change memory device further comprises a second electrode on the horizontal part.

4. The phase-change memory device of claim 3, wherein the tapering tip of the vertical part is "V" shaped.

5. The phase-change memory device of claim 3, wherein the first electrode comprises:

a recessed slope part contacting the tip of the vertical part; and

a horizontal part extending from the recessed slope part and separated from the horizontal part of the phase-change material layer by an insulation layer.

6. The phase-change memory device of claim 5, further comprising

an integrated circuit substrate;

an interlayer dielectric layer on the integrated circuit substrate;

an insulation layer on the interlayer dielectric layer and having a sloped opening therein; and

wherein the first electrode has a vertical part formed in the sloped opening to provide the recess in the first electrode.

7. The phase-change memory device of claim 6 further comprising:

a transistor formed in the integrated circuit substrate below the interlayer dielectric layer and having a source region and a drain region; and

a contact plug extending through the interlayer dielectric layer and electrically connecting the first electrode to the source region or the drain region.

8. The phase-change memory device of claim 7 further comprising an upper dielectric layer on the interlayer dielectric layer and the second electrode and a second electrode contact extending through the upper dielectric layer from the second electrode to contact an upper interconnection.

9. The phase-change memory device of claim 6, further comprising a sidewall spacer in the sloped opening that separates the vertical part of the first electrode from the insulation layer.

10. The phase-change memory device of claim 6, wherein the insulation layer includes a first layer on the interlayer dielectric layer and a second layer on the first layer and wherein the sloped opening has a sloped upper portion defined by the second layer and a substantially vertical lower portion defined by the first layer.

11. The phase-change memory device of claim 10, wherein the first layer comprises a silicon oxynitride layer and the second layer comprises a silicon oxide layer.

12. The phase-change memory device of claim 3, further comprising:

an integrated circuit substrate;

an interlayer dielectric layer on the integrated circuit substrate;

a first insulation layer on the interlayer dielectric layer and having a sloped opening having a first minimum diameter therein, the first electrode having a vertical part formed in the sloped opening and a horizontal part formed on the first insulation layer;

a second insulation layer on the first electrode and having a second opening having a maximum diameter greater than the minimum diameter of the sloped opening therein and extending to the vertical part of the first electrode, wherein the vertical part of the phase-change material layer is formed in the second opening and a horizontal part of the phase-change material layer is formed on the second insulation layer; and

a second electrode on the phase-change material layer.

13. A phase-change memory device comprising:

a semiconductor substrate;

a first insulation layer on the semiconductor substrate, the first insulation layer having a first opening defined by an upper sloped sidewall part and a bottom vertical sidewall part extending from the upper sloped sidewall part;

a first electrode disposed in the first opening and on the first insulation layer, the first electrode having a recessed slope part in the first opening and a horizontal part on the first insulation layer outside of the first opening;

a second insulation layer on the first electrode, the second insulation layer having a second opening that exposes the recessed slope part of the first electrode;

a phase-change material layer disposed in the second opening and on the second insulation layer; and

a second electrode on the phase-change material layer.

14. The phase-change memory device of claim 13, wherein the recessed slope part of the first electrode is substantially "V" shaped.

15. The phase-change memory device of claim 13, wherein:

the first insulation layer includes a stacked silicon oxynitride layer and silicon oxide layer;

the bottom vertical sidewall part of the first opening is defined by the silicon oxynitride layer; and

the upper slope sidewall part of the first opening is defined by the silicon oxide layer.

16. The phase-change memory device of claim 13, wherein a diameter of the second opening is smaller than a diameter of a bottom opening defined by the bottom vertical sidewall part of the first opening.

17. The phase-change memory device of claim 15, wherein a diameter of the second opening is smaller than a diameter of the bottom vertical sidewall part of the first opening.

18. The phase-change memory device of claim 13, wherein the phase-change material layer includes a combination of at least one material selected from the group consisting of Te and Se and another material selected from the group consisting of Pb, Sn, Ag, As, S, Si, P, O and N.

19. The phase-change memory device of claim 13, wherein:

the first insulation layer comprises a double-layer structure and includes an insulation spacer;

the double-layer structure is formed of a stacked silicon oxynitride layer and silicon oxide layer having an opening therein;

the insulation spacer is arranged on both sidewalls of the opening in the double layer structure;

an upper part of the insulation spacer is sloped and a lower part of the insulation spacer is vertical;

the upper slope sidewall of the first opening is defined by the upper sloped part of the insulation spacer; and

the bottom vertical sidewall of the first opening is defined by the bottom vertical part of the insulation spacer.

20. The phase-change memory device of claim 19, wherein a diameter of the second opening is smaller than a diameter of the bottom opening defined by the bottom vertical sidewall of the first opening.

21. A method for fabricating a phase-change memory device comprising:

forming a first insulation layer having a first opening therein on an integrated circuit substrate;

forming a first electrode on the first insulation layer, the first electrode having a vertical part including a recess in an upper portion thereof in the first opening; and

forming a phase-change material layer on the first electrode and extending into the recess.

22. The method of claim 21, wherein:

forming a first insulation layer includes patterning the first insulation layer to form the first opening, the first opening including a top opening defined by a sloped upper sidewall

part and a bottom opening defined by a substantially vertical bottom sidewall part;

forming a first electrode includes forming a conformal first electrode layer along the first insulation layer and the first opening to have a recessed slope part in the first opening;

forming a phase-change material layer comprises:

forming a second insulation layer on the first electrode layer;

patterning the second insulation layer to have a second opening exposing the recessed slope part of the first electrode layer; and

forming a phase-change material layer on the second insulation layer to fill the second opening, the method further comprising:

forming a second electrode layer on the phase-change material layer; and

sequentially patterning the second electrode layer, the phase-change material layer, the second insulation layer and the first electrode layer.

23. The method for fabricating the phase-change memory device of claim 22, wherein patterning the first insulation layer comprises:

forming an etching mask on the first insulation layer;

isotropic etching a partial thickness of the first insulation layer exposed by the etching mask to form the top opening; and then

anisotropic etching a remainder of the first insulation layer exposed by the etching mask to form a bottom opening.

24. The method for fabricating the phase-change memory device of claim 22, wherein patterning the first insulation layer comprises:

forming an etching mask on the first insulating layer;

anisotropic etching the first insulation layer exposed by the etching mask to form a temporary bottom opening having diameter of the bottom opening on the first insulation layer; and then

isotropic etching a partial thickness of the first insulation layer defining the top of the temporary bottom opening to form the top opening, wherein a residual temporary bottom opening corresponds to the bottom opening.

25. The method for fabricating the phase-change memory device of claim 23, wherein the first insulation layer is formed by sequentially stacking a silicon oxynitride layer and a silicon oxide layer, and wherein the top opening is formed in the oxide silicon layer,

and wherein the bottom opening is formed in the silicon oxynitride layer.

26. The method for fabricating the phase-change memory device of claim 24, wherein the first insulation layer is formed by sequentially stacking a silicon oxynitride layer and a silicon oxide layer and wherein the top opening is formed in the oxide silicon layer, and wherein the bottom opening is formed in the silicon oxynitride layer.

27. The method for fabricating the phase-change memory device of claim 22, wherein the second opening is formed to have a diameter smaller than a diameter of the bottom opening of the first opening.

28. The method for fabricating the phase-change memory device of claim 22, further comprising:

forming a silicon oxynitride layer and a silicon oxide layer on the second electrode layer, after forming the second electrode layer; and

patterning the silicon oxide layer and the silicon oxynitride layer while patterning the second electrode layer, the phase-change material layer, the second insulation layer and the first electrode layer.

29. The method for fabricating the phase-change memory device of claim 28, further comprising:

before forming the first insulation layer:

forming a transistor on the semiconductor substrate;

forming a first interlayer dielectric layer to cover the transistor on the semiconductor substrate; and

forming a contact pad electrically connected to a source region of the transistor and a first interconnection connected to a drain region of the transistor, and

after patterning the oxide layer, the nitride oxide layer, the second electrode layer, the phase-change material layer, the second insulation layer and the first electrode layer:

forming a protection insulation layer;

forming a second interlayer dielectric layer on the protection insulation layer;

patterning the second interlayer dielectric layer, the protection insulation layer, the patterned silicon oxide layer and the patterned silicon oxynitride layer to form a via hole exposing the patterned second electrode layer;

filling the via hole with a conductive material; and

forming a second interconnection on the second interlayer dielectric layer and the conductive material.

30. A method for fabricating a phase-change memory device, comprising:

forming a first insulation layer on a semiconductor substrate;

patterning the first insulation layer to form a temporary opening;

forming an insulation layer spacer on a sidewall of the temporary opening, the insulation layer spacer defining a first opening comprised of a top opening defined by a sloped-top lateral part and a bottom opening defined by a vertical-bottom-lateral part;

forming a first electrode layer along the first opening and the first insulation layer to have a recessed slope part in the first opening;

forming a second insulation layer on the first electrode layer;

patterning the second insulation layer to have a second opening exposing the recessed slope part of the first electrode layer;

forming a phase-change material layer in the second opening and on the second insulation layer;

forming a second electrode layer on the phase-change material layer; and

sequentially patterning the second electrode layer, the phase-change material layer, the second insulation layer and the first electrode layer.

31. The method for fabricating the phase-change memory device of claim 30, wherein the second opening is formed to have a diameter smaller than a diameter of the bottom opening of the first opening.

32. The method for fabricating the phase-change memory device of claim 30, further comprising:

forming a silicon oxynitride layer and an silicon oxide layer on the second electrode layer after forming the second electrode layer; and

patterning the silicon oxide layer and silicon oxynitride layer while sequentially patterning the second electrode layer, the phase-change material layer, the second insulation layer and the first electrode layer.

33. The method for fabricating the phase-change memory device of claim 32,

further comprising:

before forming the first insulation layer:

forming a transistor on the semiconductor substrate;

forming a first interlayer dielectric layer to cover the transistor on the semiconductor substrate; and

forming a contact pad electrically connected to a source region of the transistor and a first interconnection connected to a drain region of the transistor, and

after sequentially patterning the silicon oxide layer, the silicon oxynitride layer, the second electrode layer, the phase-change material layer, the second insulation layer and the first electrode layer:

forming a protection insulation layer;

forming a second interlayer dielectric layer on the protection insulation layer;

patterning the second interlayer dielectric layer, the protection insulation layer, the patterned oxide silicon layer and the silicon oxynitride layer to form a via hole exposing the patterned second electrode layer;

filling the via hole with a conductive material; and

forming a second interconnection on the second interlayer dielectric layer and the conductive material.